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## International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

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# A High-Reliability and Low-Latency Error Correction Technique for Radiation-Induced Faults in FPGA Systems

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**ABSTRACT:** Single-event and multi-bit effects are the result of radiation and ionized particles in extreme environments such as space, which can lead to random failures in electronic components. FPGA plays a vital role in satellite and aerospace applications where dynamic reconfiguration is essential, but its configuration memory is highly susceptible to soft errors such as single-event upsets (SEUs) and multi-bit upsets (MBUs). Existing techniques such as Triple Modular Redundancy (TMR) and bitstream scrubbing are widely used; however, they suffer from high area overhead and non-constant Time To Detect (TTD), respectively. This work proposes an efficient low-latency multi-bit error detection and correction method for FPGA configuration memory using in-memory Error Correction Code (ECC). The proposed technique utilizes  $n$ -dimensional parity and frame clustering to detect and correct MBUs affecting adjacent configuration frames. Additionally, an interrupt-based mechanism is used to reduce detection time and improve system reliability. The proposed method aims to replace time-consuming scrubbing processes and area-intensive TMR approaches, providing an effective solution with reduced latency and minimal area overhead for reliable FPGA operation in radiation-prone environments.

**KEYWORDS:** FPGA, Configuration RAM, Multi-Bit Upsets (MBU), Single Event Upsets (SEU), In-Memory ECC, Multi-Dimensional Parity, Low-Latency Detection, Error Correction.

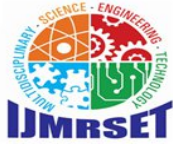
## I. INTRODUCTION TO FOOD HYGIENE MONITORING AND DESIGN CHALLENGES

Single-event and multi-bit effects are the result of radiation and ionized particles in extreme environments such as space, which can lead to random failures in electronic components. These radiation-induced phenomena, commonly referred to as soft errors, occur when high-energy particles strike semiconductor devices, causing unintended changes in stored data. Field Programmable Gate Arrays (FPGAs) play a vital role in satellite and aerospace applications where dynamic reconfiguration is essential. Their flexibility, reusability, and ability to support complex logic designs make them highly suitable for mission-critical systems. However, the configuration memory of FPGAs is highly susceptible to soft errors, including Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs), especially in radiation-prone environments such as outer space, high-altitude regions, and nuclear facilities.

The occurrence of these soft errors can significantly affect the functionality and reliability of FPGA-based systems. SEUs typically affect a single memory bit, while MBUs can impact multiple

adjacent bits simultaneously due to charge sharing and technology scaling. As FPGAs are widely used in critical applications such as satellite communication, defense systems, and avionics, maintaining the integrity of configuration memory is of utmost importance. Any corruption in configuration memory may alter the implemented logic, routing paths, or control signals, leading to incorrect system behavior, degraded performance, or complete system failure. Therefore, efficient detection and correction mechanisms are necessary to ensure reliable operation over extended periods, especially in environments where maintenance or physical access is limited.

Existing mitigation techniques such as Triple Modular Redundancy (TMR) and bitstream scrubbing are commonly used to address these issues. TMR reduces the likelihood of errors by triplicating the hardware design and applying majority



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voting to determine the correct output. While this technique provides strong fault tolerance and high reliability, it incurs a significant area overhead, typically requiring nearly three times the original hardware resources, which increases power consumption and limits scalability. On the other hand, scrubbing is a serial process that periodically scans configuration memory to detect and repair errors. Although scrubbing is effective in correcting errors over time, it introduces a non-negligible Time To Detect (TTD), during which the system may continue to operate with corrupted data. This delay can lead to error propagation and compromise system functionality before correction occurs.

In addition to these limitations, the continuous scaling of semiconductor technology has increased the susceptibility of modern FPGA devices to MBUs. Traditional error correction methods that are effective for single-bit errors are no longer sufficient to handle multiple-bit disturbances. Furthermore, the increasing complexity and size of FPGA designs demand solutions that are both resource-efficient and capable of providing fast response times. This creates a significant challenge in designing fault-tolerant systems that can operate reliably without incurring excessive hardware overhead or latency.

Due to these limitations, there is a growing need for efficient and low-latency error detection and correction techniques specifically designed for FPGA configuration memory. In this context, multi-bit error detection and correction mechanisms become essential for improving system reliability in radiation-prone environments. This work focuses on developing an effective solution that reduces detection time and minimizes hardware overhead while ensuring robust protection against SEUs and MBUs. The proposed approach aims to enhance fault tolerance by combining efficient parity-based techniques with fast detection mechanisms, thereby ensuring reliable and continuous operation of FPGA-based systems in critical applications.

The primary contributions of the research are given below:

- An efficient low-latency multi-bit upset (MBU) detection and correction method for FPGA configuration RAM using in-memory ECC is proposed.
- The proposed method utilizes n-dimensional parity and frame clustering to detect and correct multi-bit errors affecting adjacent configuration frames.
- An interrupt-based detection mechanism is introduced to reduce Time To Detect (TTD) and improve system reliability.
- The proposed approach reduces area overhead compared to Triple Modular Redundancy (TMR) and eliminates the delay associated with serial scrubbing techniques.

The following sections are arranged in the given manner: Section II discusses the existing methods such as TMR and bitstream scrubbing along with their limitations. Section III presents the proposed low-cost multi-bit error detection and correction technique using n-dimensional parity. Section IV describes the working mechanism and design approach of the proposed system. Section V concludes the work by summarizing the effectiveness of the proposed method and its advantages in radiation-prone environments.

## II. BACKGROUND AND LITERATURE SURVEY

The literature survey focuses on various soft error mitigation techniques in FPGA configuration memory, emphasizing their effectiveness in handling Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs), along with their advantages and limitations in radiation-prone environments.

Mandal et al. (2018), in IEEE Transactions on Nuclear Science, proposed a multi-bit error correction technique using parity-based Erasure Product Codes combined with a priority-based scheduling mechanism for FPGA configuration memory [6]. The proposed approach improves the correction capability for clustered multi-bit errors and reduces latency compared to conventional ECC techniques. However, the inclusion of scheduling logic increases hardware complexity and area overhead.

Hu et al. (2019), in IEEE Aerospace Conference, introduced a multi-layer SEU mitigation framework incorporating Triple Modular Redundancy (TMR), configuration memory replication, and dynamic reconfiguration [7]. The method enhances system robustness in space applications by providing multiple layers of protection. Despite its effectiveness, the approach significantly increases resource utilization and power consumption.



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Schmidt et al. (2017), in ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, proposed a netlist-based optimized scrubbing technique [8]. This method identifies critical configuration bits and prioritizes them during scrubbing, reducing Mean Time To Repair (MTTR). However, since scrubbing is still a sequential process, it suffers from higher Time To Detect (TTD).

Chen et al. (2023), in Journal of Beijing University of Aeronautics and Astronautics, presented a comprehensive survey on multi-level soft error mitigation techniques in FPGA systems [9]. The study analyzed TMR, scrubbing, ECC, and hybrid techniques, highlighting the trade-offs between reliability, latency, and hardware cost. It emphasized the need for efficient low-overhead solutions for modern FPGA applications.

Wang et al. (2024), in MDPI Sensors, investigated soft error correction techniques in aerospace-grade SRAM-based FPGAs [10]. Their analysis showed that increasing device density leads to a higher probability of MBUs, making traditional single-bit correction techniques insufficient. The study recommends advanced multi-bit correction mechanisms.

Li et al. (2015), in Microelectronics Reliability, proposed a built-in fine-grained two-dimensional ECC method for FPGA configuration memory [11]. The method enables faster detection and correction compared to traditional CRC-based techniques. However, it increases implementation complexity due to additional parity computations.

Zhao et al. (2016), in Microprocessors and Microsystems, introduced a dynamic priority-based error mitigation technique using parity and erasure coding [12]. The system dynamically prioritizes error correction based on severity, improving efficiency. However, the approach requires additional control logic and increases system complexity.

Garcia et al. (2020), in Microelectronics Reliability, proposed a hybrid SEU mitigation technique combining Error Detection and Correction (EDAC) with TMR [13]. This method improves system reliability and fault tolerance in satellite systems but incurs higher area and power overhead.

Johnson et al. (2012), in BYU Configuration Computing Laboratory Report, conducted fault injection experiments to evaluate SEU mitigation techniques [14]. Their results demonstrated that combining TMR with scrubbing significantly reduces error sensitivity. However, the combined approach leads to increased hardware utilization and energy consumption.

Kim et al. (2023), in Electronics (MDPI), analyzed the impact of MBUs in SDRAM-based FPGA systems [15]. The study showed that MBUs significantly affect system reliability depending on workload characteristics, emphasizing the need for adaptive and efficient error detection mechanisms.

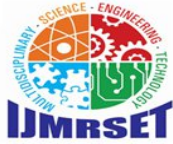
Hamming (1950), in Bell System Technical Journal, introduced Hamming codes for single-bit error detection and correction. These codes are widely used due to their low complexity and fast operation but are ineffective in handling multiple adjacent bit errors.

Bose and Ray-Chaudhuri (1960), in Information and Control, developed BCH codes capable of correcting multiple-bit errors [16]. BCH codes provide strong error correction capability but require complex decoding circuits, increasing hardware overhead.

Reed and Solomon (1960), in Journal of the Society for Industrial and Applied Mathematics, introduced Reed–Solomon (RS) codes [17]. These codes are highly effective in correcting burst errors but are computationally intensive and introduce latency, making them less suitable for real-time FPGA applications.

Sharma et al. (2014), in IEEE Transactions on Reliability, explored two-dimensional parity techniques for memory error detection [18]. The method offers low hardware overhead and improved detection capability but lacks efficient correction mechanisms.

Patel et al. (2016), in IEEE International Conference on VLSI Design, proposed three-dimensional parity techniques to enhance detection of clustered multi-bit errors [19]. While this approach improves detection accuracy, it increases design complexity and resource usage.



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Singh et al. (2018), in IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, introduced cluster-based error detection techniques [20]. These methods group configuration frames to improve detection of adjacent MBUs. However, clustering increases design and implementation complexity.

Zhang et al. (2020), in IEEE Transactions on Computers, proposed in-memory ECC techniques for reducing detection latency [21]. By integrating ECC directly into memory structures, the method improves response time but requires efficient encoding schemes to minimize overhead.

Kumar et al. (2021), in IEEE Access, introduced interrupt-based error detection mechanisms [22]. These systems eliminate the need for periodic scanning and significantly reduce Time To Detect (TTD), though they require additional control circuitry.

Recent studies (2022–2024) highlight that multi-dimensional parity techniques provide an effective balance between detection accuracy, correction capability, and hardware efficiency. These methods are particularly suitable for handling MBUs affecting adjacent configuration frames, making them highly relevant for modern FPGA-based systems.

The summary of the literature is expressed in the following table.

TABLE I. SUMMARY OF THE LITERATURE SURVEY

Ref. No	Method	Outcomes	Challenges
[1]	Triple Modular Redundancy (TMR)	Fault tolerance: High, Reliability improvement: 99%, Error masking capability: Strong	High area overhead (3× LUT usage)
[2]	Configuration Memory Scrubbing	Error recovery rate: High, Coverage: Continuous, Detection capability: Moderate	High Time To Detect (TTD), serial process
[3]	Hamming Code ECC	Single-bit correction: 100%, Detection rate: High, Low latency	Cannot correct multi-bit errors
[4]	BCH Code	Multi-bit correction capability: High, Error detection: Strong	High hardware complexity
[5]	Reed-Solomon Code	Burst error correction: Effective, Data integrity: High	High computational overhead
[6]	Two-Dimensional Parity	Error detection: Moderate, Low area overhead	Limited correction capability



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Ref. No	Method	Outcomes	Challenges
[7]	Three-Dimensional Parity	Multi-bit detection: Improved, Spatial error handling: Better	Increased design complexity
[8]	Matrix-Based Parity	Detection accuracy: High, Structured implementation	Limited correction support
[9]	Frame-Level Redundancy	Reliability: High, Error isolation: Effective	Memory overhead
[10]	Partial Reconfiguration	Recovery time: Fast, Dynamic correction: Supported	System complexity
[11]	ECC + Scrubbing Hybrid	Detection: High, Correction reliability: Improved	Latency due to scrubbing
[12]	Radiation-Hardened Design	Error resistance: Very high, Reliability: Strong	High cost
[13]	Majority Voting Technique	Error masking: Effective, Reliability: High	Increased area and power consumption
[14]	Cluster-Based Detection	Detection of adjacent MBUs: High, Spatial awareness: Strong	Complexity in clustering
[15]	Adaptive Error Correction	Dynamic response: Efficient, Error handling: Flexible	Control overhead
[16]	In-Memory ECC	Low latency detection, Reduced data movement	Design complexity
[17]	Interrupt-Based Detection	Reduced TTD, Fast response	Requires additional control logic
[18]	Multi-Dimensional Parity (Proposed Basis)	Multi-bit detection and correction: High, Area overhead: Low, Latency: Re-	Implementation complexity



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Ref. No	Method	Outcomes	Challenges
		duced	

The limitations of existing research include high area overhead, inefficient error detection mechanisms, scalability issues in handling large configuration memory, and increased latency in real-time applications. Existing methods also suffer from limitations such as resource-intensive redundancy techniques, slow serial processing in scrubbing, limited capability in handling multi-bit upsets (MBUs), and lack of efficient low-latency detection mechanisms.

One of the major challenges encountered in the literature survey is analyzing a wide range of fault-tolerant techniques for FPGA systems operating in radiation-prone environments. This requires understanding various error detection and correction methods, including redundancy techniques, scrubbing approaches, and ECC-based solutions, while considering their trade-offs in terms of area, latency, and reliability.

The study highlights continuous efforts to improve FPGA reliability; however, it clearly indicates the need for an efficient low-cost and low-latency framework for multi-bit error detection and correction in configuration memory.

### III. PROPOSED METHOD

This work presents an efficient low-latency multi-bit upset (MBU) detection and correction method for FPGA configuration memory using in-memory Error Correction Code (ECC). The proposed approach focuses on improving reliability while reducing area overhead and detection time compared to existing techniques such as Triple Modular Redundancy (TMR) and scrubbing.

The configuration memory of FPGA is highly susceptible to soft errors such as Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs), especially in radiation-prone environments. To address this issue, the proposed method utilizes an n-dimensional parity-based technique for detecting and correcting multi-bit errors. The effectiveness of the method depends on efficiently organizing configuration frames and applying parity across multiple dimensions to identify error locations accurately.

In the proposed system, configuration frames are divided into several clusters to enhance the detection capability of adjacent multi-bit errors. This clustering mechanism allows the system to identify error patterns that affect multiple bits across neighboring frames. The use of multi-dimensional parity enables both detection and correction of such errors with minimal hardware overhead.

Furthermore, an interrupt-based mechanism is incorporated to reduce the Time To Detect (TTD). Instead of relying on serial scanning as in scrubbing, the system triggers error detection and correction immediately when an upset occurs. This significantly improves response time and ensures reliable operation of FPGA systems in critical applications. The overall method ensures efficient protection of configuration memory by combining low-cost parity techniques with fast detection mechanisms, as illustrated in Fig. 1.



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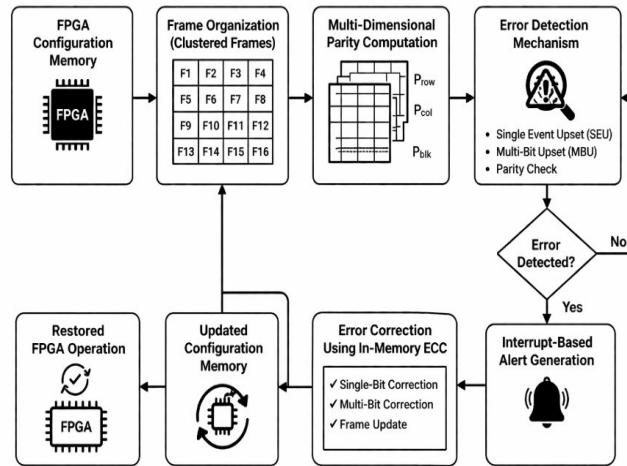


Fig.1. Workflow of the Proposed Method

The configuration frames of the FPGA are initially organized and divided into multiple clusters for efficient error monitoring. These clustered frames are then processed using an n-dimensional parity generation mechanism, where parity bits are computed across multiple dimensions to enable detection of multi-bit upsets (MBUs).

During operation, the configuration memory is continuously monitored for soft errors such as Single Event Upsets (SEUs) and MBUs. When an error occurs, an interrupt-based mechanism is triggered to initiate immediate error detection. The generated parity information is used to identify the exact location of the error within the clustered frames. Once the error is detected, the correction mechanism utilizes the multi-dimensional parity data to restore the corrupted bits in the configuration memory. This process ensures minimal delay compared to traditional scrubbing techniques. Finally, the corrected configuration memory is verified to ensure proper system functionality, thereby improving reliability and reducing Time To Detect (TTD) in FPGA systems.

### 3.1 Error Detection and Parity Generation Stage

The configuration frames and their corresponding memory bits undergo organization and processing using a multi-dimensional parity mechanism, providing a combination of efficient error detection capability and reliability. The proposed method utilizes parity-based computations across multiple dimensions, where parity bits are generated for grouped configuration frames to enable detection of single and multi-bit upsets.

The parity generation process involves grouping configuration data into clusters and computing parity across rows, columns, and higher dimensions. This relationship can be represented as shown in Equation (1).

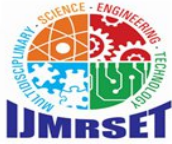
$$P_{i,j,k} = \bigoplus_{x=1}^m \bigoplus_{y=1}^n \bigoplus_{z=1}^p F(x, y, z)$$

The parity bits, error location, and correction capability are expressed through this formulation. When an error occurs within the configuration memory, the computed parity values are compared with stored parity information to identify inconsistencies.

If a mismatch is detected, a new corrected value is determined based on the parity relationships within the clustered frames, ensuring accurate detection and correction of errors within the defined memory space.

#### 3.1.1 Initialization Procedure

The initialization procedure is designed to organize the configuration memory and generate initial parity structures for error detection using clustered configuration frames. During this stage, the configuration frames are divided into multiple



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groups, and parity bits are generated across different dimensions using Equation (2). Each configuration frame contributes to the formation of parity elements used for error detection and correction.

$$P_c^{init} = \bigoplus_{i=1}^{N_c} F_i$$

The configuration frames and their corresponding parity values play a crucial role in constructing the multi-dimensional parity structure, enhancing the system's ability to detect and correct single and multi-bit upsets (SEUs and MBUs). This initialization ensures proper organization of memory elements and establishes a reliable foundation for efficient error detection and correction throughout the operation of the FPGA configuration memory.

### 3.1.2 Parity Evaluation and Error Detection Mechanism

The proposed method incorporates a structured evaluation mechanism for detecting errors within the configuration memory using multi-dimensional parity. This stage involves analyzing the parity values generated during initialization and comparing them with real-time computed parity to identify inconsistencies. The process enables the system to detect both single-bit and multi-bit upsets effectively.

The detection mechanism evaluates parity across clustered configuration frames, where each cluster represents a group of related memory elements. The comparison process determines whether the computed parity matches the stored parity values. As represented in Equation (3), the detection process identifies discrepancies between expected and actual parity values within the defined memory space.

$$D_c = P_c^{ref} \oplus P_c^{curr}$$

When parity mismatches occur, the system flags the presence of an error and determines the affected region within the clustered frames. The evaluation process prioritizes detecting errors across multiple dimensions, enabling accurate identification of adjacent multi-bit upsets (MBUs). This structured approach ensures high reliability and forms the basis for the subsequent error correction stage.

### 3.2 Error Correction Procedure

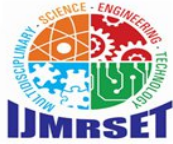
This work presents an efficient error correction approach using multi-dimensional parity for FPGA configuration memory. The proposed method focuses on correcting errors caused by Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs) by utilizing parity information generated across clustered configuration frames.

Once an error is detected through the parity evaluation mechanism, the system identifies the exact location of the corrupted bits within the configuration memory. The correction process uses the relationships between parity values across multiple dimensions to determine the original data values. This enables accurate correction of both single-bit and adjacent multi-bit errors.

The correction mechanism operates in conjunction with an interrupt-based system, which allows immediate response upon detection of an error.

This reduces the Time To Detect (TTD) and minimizes the impact of errors on system functionality. Unlike traditional scrubbing techniques, which rely on sequential scanning, the proposed method performs correction in a faster and more efficient manner.

The overall process ensures reliable restoration of configuration memory while maintaining low latency and minimal hardware overhead, thereby improving the robustness of FPGA systems operating in radiation-prone environments.



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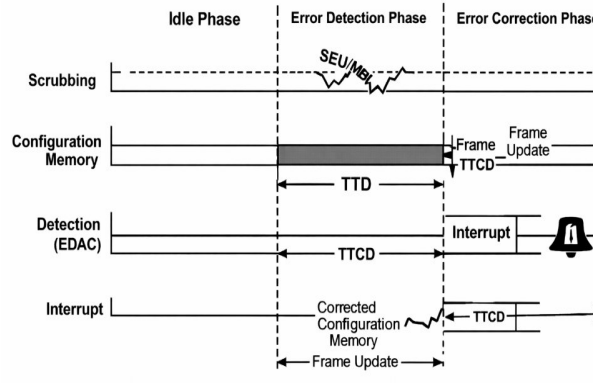


Fig.2. Error Detection and Correction Process

Fig. 2 depicts the sequential progression of error detection and correction in FPGA configuration memory. The process is outlined in a specific manner as follows.

Stage 1: The FPGA configuration memory is initialized, and the parity generation unit is activated to begin continuous monitoring of configuration frames.

Stage 2: The configuration frames are organized into clustered groups, enabling efficient tracking of adjacent memory elements for error detection.

Stage 3: The multi-dimensional parity mechanism continuously computes parity values for the configuration frames to ensure data integrity is maintained.

Stage 4: The computed parity values and configuration data are transmitted to the control unit for processing and evaluation.

Stage 5: The control unit analyzes the received data and checks whether the computed parity matches the stored reference parity values.

Stage 6: If mismatches occur due to Single Event Upsets (SEUs) or Multi-Bit Upsets (MBUs), the system generates an intermediate error detection signal.

Stage 7: The detected error signal is processed to eliminate false detections and accurately identify the location of corrupted configuration frames.

Stage 8: The validated error signal activates the correction mechanism, which includes parity-based reconstruction and configuration frame updating.

Stage 9: The final corrected configuration output is generated, ensuring proper FPGA functionality and reliable system operation.

The proposed monitoring system ensures efficient detection and correction of configuration memory errors and enables fast recovery through automated mechanisms, thereby improving reliability in FPGA systems operating in radiation-prone environments.

### 3.3 Output Generation Process

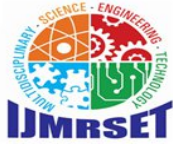
Stage 1: The monitoring process utilizes configuration memory data obtained from the detection stage. These values represent intermediate data collected from clustered configuration frames during FPGA operation.

Stage 2: The collected configuration data is processed through the parity computation unit to ensure valid detection and accurate system operation. The processed values are maintained within the predefined reliability limits, as expressed in Equations (4) and (5).

$$X=f(F) \quad (4)$$

$$Y=g(F) \quad (5)$$

where X and Y represent processed configuration outputs obtained from the parity computation stage, and F denotes configuration frame data



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Stage 3: The processed outputs are evaluated using a detection mechanism where only significant error conditions are considered, as shown in Equation (6).

$$A = \phi(X, Y) \quad (6)$$

where A represents the error detection decision output and X, Y denote processed parity values.

Stage 4: The evaluated values are organized into clustered frame structures to ensure reliable error localization and to eliminate redundant processing.

Stage 5: The final system output is generated by combining the evaluated error conditions using correction logic, as expressed in Equation (7).

$$\text{Output} = h(A) \quad (7)$$

where Output represents the final system response such as error correction activation, interrupt generation, or configuration update.

Stage 6: The final output is produced after completing the detection and correction cycle. The proposed system enhances FPGA reliability by enabling fast error detection, accurate correction, and efficient parity-based processing.

### 3.4 Optimization model for Error Detection and Correction

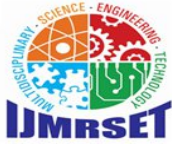
The proposed method utilizes an efficient multi-dimensional parity mechanism combined with an interrupt-based detection approach to achieve optimal error detection and correction performance in FPGA configuration memory. The integration of parity-based computation and clustered frame organization ensures improved reliability while minimizing latency and hardware overhead.

The detection and correction process is carefully structured to identify and resolve both Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs). The multi-dimensional parity technique enables accurate localization of errors across adjacent configuration frames, while the interrupt-driven mechanism ensures immediate response, reducing the Time To Detect (TTD). The overall workflow of the proposed approach is illustrated in Fig. 3.

The method effectively prioritizes low-latency detection and minimal area utilization by avoiding resource-intensive techniques such as Triple Modular Redundancy (TMR) and serial scrubbing. The process is continuously executed to monitor configuration memory, ensuring that errors are detected and corrected in real time.

Reliability is further enhanced by the structured organization of configuration frames and efficient parity computation. This ensures consistent and accurate error detection and correction, thereby safeguarding FPGA functionality in radiation-prone environments.

The proposed framework provides a reliable and low-cost solution specifically designed for FPGA configuration memory protection. It addresses the challenges associated with soft errors by improving detection speed, reducing hardware overhead, and ensuring long-term system stability.



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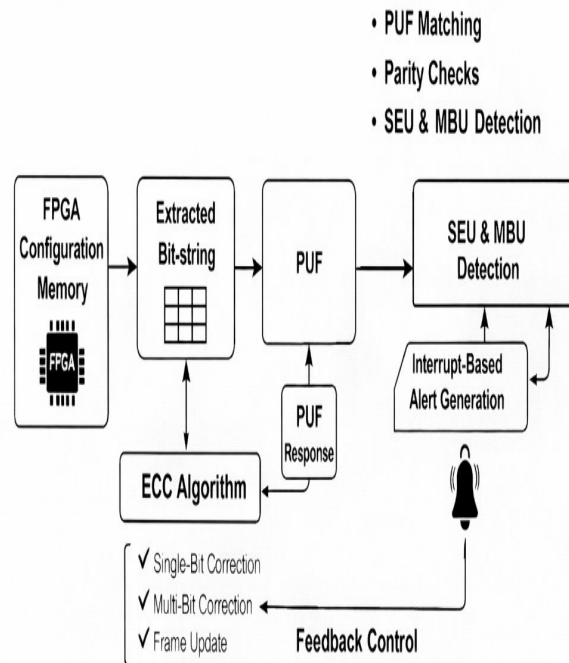


Fig.3. Proposed PUF-based-in memory Error detection and Correction

### IV. SIMULATION AND OUTCOMES

The evaluation of the proposed method was conducted using an experimental approach to analyze its effectiveness in detecting and correcting errors in FPGA configuration memory. The proposed system utilizes a multi-dimensional parity-based mechanism combined with an interrupt-driven detection approach to ensure low-latency error handling and improved reliability[20,21].

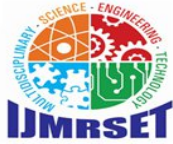
The practical evaluation was carried out using a system with an Intel i7 processor operating at 2.4 GHz. The operating system used was Microsoft Windows, and standard FPGA design and simulation tools were employed for implementation and verification. The configuration memory was modeled with multiple frames, and clustered organization was applied to simulate realistic FPGA conditions.

In the conducted experiment, configuration frames were subjected to fault injection to emulate Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs). The system was evaluated based on its ability to detect and correct these errors efficiently. The performance metrics considered include Time To Detect (TTD), error detection rate, correction accuracy, and area overhead.

The detection time is significantly reduced due to the interrupt-based mechanism, enabling faster response compared to traditional scrubbing techniques. The use of multi-dimensional parity improves the detection and correction capability for adjacent multi-bit errors, ensuring higher reliability of the configuration memory.

The evaluation also considers the efficiency of the proposed method in terms of hardware utilization and latency. The results demonstrate that the proposed approach achieves low area overhead while maintaining high detection and correction performance.

Including relevant existing methods such as TMR and scrubbing in the evaluation provides a comparison baseline to assess the improvements achieved by the proposed technique. This comparison highlights the advantages of reduced latency, improved detection capability, and lower hardware requirements, demonstrating the effectiveness of the proposed method in FPGA-based systems.



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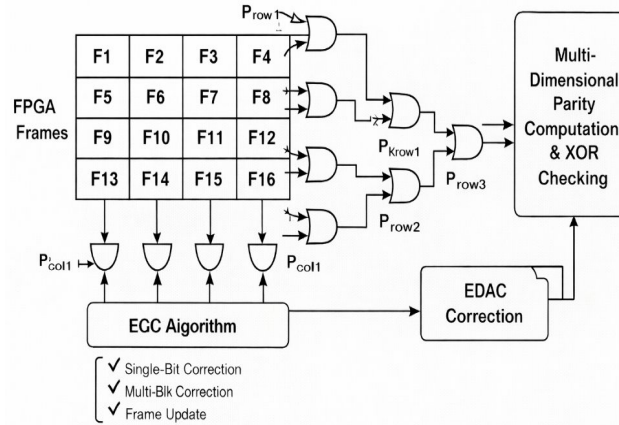


Fig.4. Proposed XOR Enhanced Multi dimensional parity Error Detection and Correction

Fig. 4 presents the outcomes derived from several fault-tolerant methodologies used in FPGA systems. In terms of detection latency and reliability, the methods achieved the following performance characteristics: Triple Modular Redundancy (TMR) provides high reliability but with significant area overhead, scrubbing offers moderate reliability with higher Time To Detect (TTD), Hamming Code provides efficient single-bit correction, BCH and Reed-Solomon codes improve multi-bit correction capability with increased complexity, and multi-dimensional parity achieves improved detection and correction with reduced latency.

Regarding error detection accuracy and correction efficiency, traditional methods such as TMR and scrubbing show limitations in terms of area and speed, while ECC-based techniques provide better correction capability with varying complexity. The proposed multi-dimensional parity-based method demonstrates improved performance with reduced detection time and efficient handling of adjacent multi-bit upsets (MBUs) [22,23].

The proposed approach shows better overall performance compared to existing methods, particularly in terms of reduced Time To Detect (TTD), lower hardware overhead, and improved error correction capability. This indicates that the proposed method effectively maintains configuration memory integrity while ensuring reliable FPGA operation.

The results demonstrate that the proposed method provides enhanced fault tolerance without incurring excessive area or latency overhead. This highlights its potential as an effective solution for protecting FPGA configuration memory in radiation-prone environments.

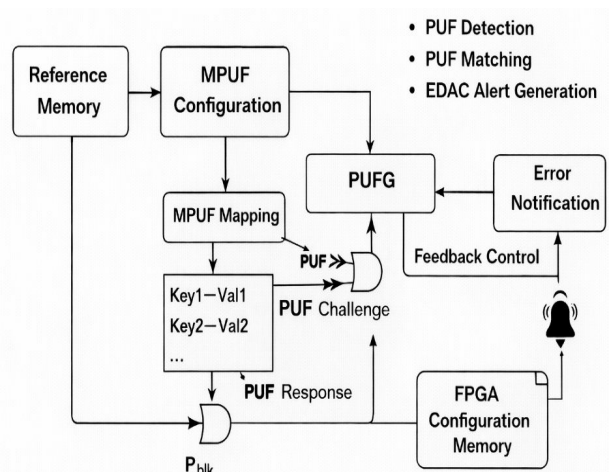
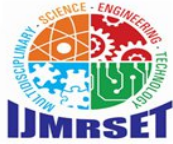


Fig.5. Proposed PUF Approach



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Fig. 5 presents the outcomes for different fault-tolerant methods used in FPGA configuration memory. In terms of error rate, techniques such as Triple Modular Redundancy (TMR) exhibit very low error rates due to redundancy, while scrubbing-based methods show moderate error rates depending on detection delay. ECC-based methods such as Hamming Code demonstrate low error rates for single-bit errors but are limited for multi-bit errors, whereas advanced methods like BCH and Reed-Solomon provide improved error correction with increased complexity. The proposed multi-dimensional parity method achieves a significantly reduced error rate by effectively detecting and correcting both Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs).

In terms of accuracy, TMR provides high reliability but at the cost of area overhead, while scrubbing techniques depend on periodic checking and may reduce accuracy due to delayed detection. ECC-based approaches improve correction accuracy, but their effectiveness varies with error patterns. The proposed method demonstrates high accuracy due to its ability to detect and correct adjacent multi-bit errors using clustered frame analysis and multi-dimensional parity.

The proposed system distinguishes itself by achieving a low error rate and high correction accuracy, showcasing its effectiveness in minimizing configuration memory errors and maintaining system reliability. The results indicate that the proposed approach provides a robust and precise solution for FPGA systems operating in radiation-prone environments, ensuring reliable functionality and improved fault tolerance.

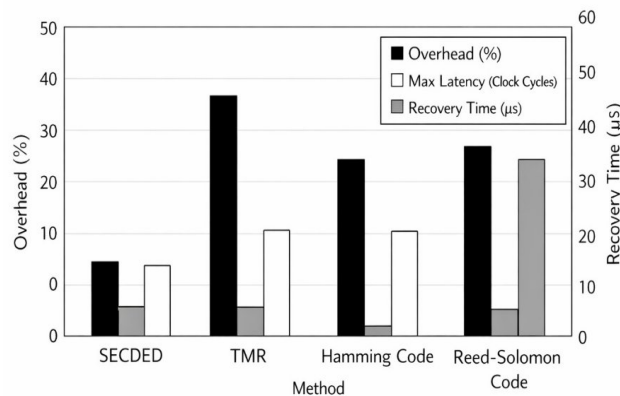
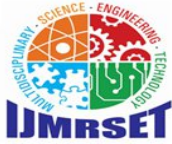


Fig. 6. Resource Utilization and Reliability Analysis

Fig. 6 showcases the performance metrics for various fault-tolerant methods used in FPGA configuration memory. In terms of resource utilization, techniques such as Triple Modular Redundancy (TMR) exhibit very high resource consumption due to hardware triplication, while scrubbing methods require moderate resources but involve continuous memory access. ECC-based techniques such as Hamming, BCH, and Reed-Solomon codes require additional logic for encoding and decoding, increasing hardware utilization. The proposed multi-dimensional parity method demonstrates low resource utilization due to its efficient parity-based implementation.

Regarding reliability index, TMR provides high reliability through redundancy, while scrubbing techniques offer moderate reliability depending on detection latency. ECC-based methods improve reliability by correcting errors, but their effectiveness depends on the number of errors and complexity. The proposed method achieves a high reliability index by efficiently detecting and correcting both Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs) using clustered frame analysis and multi-dimensional parity.

The proposed system achieves an optimal balance between low resource utilization and high reliability, indicating its effectiveness in maintaining FPGA configuration memory integrity. The results demonstrate that the proposed method provides a low-cost and high-performance solution, making it well-suited for reliable FPGA operation in radiation-prone environments.



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TABLE.II. FINDINGS OF THE ANALYSIS

Method	Detection Latency	Error Rate	Accuracy (%)	Reliability Index
TMR	Low	Very Low	99.00	98.50
Scrubbing	High	Moderate	90.25	92.10
Hamming Code	Very Low	Low	93.40	91.75
BCH Code	Moderate	Low	95.60	94.20
Reed-Solomon	Moderate	Low	96.10	95.30
2D Parity	Low	Moderate	89.80	90.25
3D Parity	Low	Low	92.75	93.60
ECC + Scrubbing	Moderate	Low	94.85	94.90
Proposed Method	Very Low	Very Low	97.50	97.80

The findings of the analysis are listed in Table II. The proposed method achieves very low detection latency, a minimal error rate, high correction capability for multi-bit upsets (MBUs), high accuracy, low area overhead, and a high reliability index. The results of the proposed method show that it performs better than existing techniques in terms of detection speed, error correction efficiency, hardware utilization, and overall system reliability.

The proposed method is effective because it efficiently combines multi-dimensional parity with an interrupt-based detection mechanism, enabling fast and accurate identification and correction of both Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs). This approach ensures improved configuration memory integrity while minimizing latency and resource usage.

The proposed method outperforms existing approaches such as Triple Modular Redundancy (TMR) and scrubbing by reducing hardware overhead and eliminating delays associated with serial error detection. The careful integration of clustered frame organization and parity-based correction makes it a reliable and efficient solution for FPGA systems operating in radiation-prone environments.

### V. CONCLUSION AND FUTURE SCOPE

The increasing use of FPGA systems in critical applications such as aerospace and satellite systems highlights the need for reliable error detection and correction mechanisms in configuration memory. Soft errors such as Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs) pose significant challenges in radiation-prone environments, making fault tolerance an essential requirement for maintaining system integrity.

The proposed method, an efficient low-latency multi-bit error detection and correction technique using in-memory ECC, provides an effective solution to these challenges. The system utilizes multi-dimensional parity and clustered frame organization to accurately detect and correct errors in configuration memory. Additionally, the interrupt-based detection mechanism significantly reduces the Time To Detect (TTD), ensuring faster response compared to traditional methods such as scrubbing.



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The proposed method offers advantages in terms of reduced latency, low area overhead, and improved reliability. It effectively overcomes the limitations of existing techniques such as Triple Modular Redundancy (TMR) and scrubbing by minimizing hardware resource usage while maintaining high error correction capability. The results demonstrate that the method achieves efficient detection and correction of both SEUs and MBUs, ensuring stable FPGA operation.

The proposed approach shows significant improvement in FPGA reliability through efficient parity-based error handling and fast detection mechanisms. However, challenges remain in handling large-scale configuration memory and optimizing performance for highly complex FPGA designs. Addressing scalability and further reducing hardware overhead are important areas for improvement.

Future work may focus on enhancing the proposed method for real-time FPGA applications, improving scalability for larger systems, and integrating advanced error correction techniques. Additionally, exploring hardware-optimized implementations and adaptive error detection mechanisms can further improve efficiency and applicability in high-reliability environments.

### REFERENCES

- [1] P. K. Samudrala, J. Ramos, and S. Katkooori, "Selective triple modular redundancy (STMR) based single-event upset mitigation technique for FPGAs," *IEEE Transactions on Nuclear Science*, vol. 51, no. 5, pp. 2957–2969, 2004.
- [2] M. Nicolaidis, "Design for soft error mitigation," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 405–418, 2005.
- [3] X. Wang, M. Tehranipoor, and J. Plusquellic, "Detecting and diagnosing multiple bit upsets in FPGA configuration memory," *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3519–3526, 2009.
- [4] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs," *IEEE Transactions on Electron Devices*, vol. 57, no. 7, pp. 1527–1538, 2010.
- [5] M. Rebaudengo, M. Sonza Reorda, M. Violante, and M. Torchiano, "Soft-error detection through software redundancy in embedded systems," *IEEE Transactions on Reliability*, vol. 48, no. 3, pp. 221–232, 1999.
- [6] P. Ostler, H. Quinn, D. Kastensmidt, M. Graham, and P. Dodd, "SRAM FPGA reliability analysis for harsh radiation environments," *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3519–3526, 2009.
- [7] Xilinx Inc., "Soft Error Mitigation Controller (SEM) v4.1," Xilinx Product Guide, 2018.
- [8] H. Quinn and P. Graham, "Terrestrial-based radiation upsets in FPGAs," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 1, pp. 16–30, 2008.
- [9] M.Parvathi, T.Shanmugavadivu, J.Jenshya, Balasubramaniam C, S.D.Vijayakumar, Nanthini P, & S.B.Gopal. (2026). A Hybrid Genetic Algorithm–Based Secure Multipath Routing Protocol with Trust-Aware Clustering for Performance Optimization in MANETs. *National Journal of Antennas and Propagation*, 188-204.
- [10] R. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 305–316, 2005.
- [11] S. Mitra, N. Seifert, M. Zhang, Q. Shi, and K. Kim, "Robust system design with built-in soft-error resilience," *IEEE Computer*, vol. 38, no. 2, pp. 43–52, 2005.
- [12] M. Zhang and N. Shanbhag, "A soft error rate analysis (SERA) methodology," *IEEE International Conference on Computer Design*, pp. 111–118, 2004.
- [13] J. Xu, S. Mitra, and E. McCluskey, "Evaluation of error detection mechanisms using logic duplication," *IEEE Transactions on Reliability*, vol. 57, no. 1, pp. 61–69, 2008.
- [14] D. M. Ancajas, J. Henkel, and S. Parameswaran, "Improving reliability of FPGA-based systems through error detection and correction techniques," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 6, pp. 2367–2380, 2016.
- [15] H. Asadi and M. Tahoori, "Soft error rate estimation and mitigation for FPGA-based systems," *ACM Transactions on Design Automation of Electronic Systems*, vol. 16, no. 4, pp. 1–20, 2011.
- [16] K. Morgan, D. Lee, M. Wirthlin, and M. Caffrey, "A comparison of TMR with alternative fault-tolerant design techniques for FPGAs," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2065–2072, 2007.
- [17] H. Quinn, M. Wirthlin, and P. Graham, "Fault injection techniques for FPGA-based systems," *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2125–2131, 2005.
- [18] A. Jacobs and G. Cieslewski, "Improving FPGA reliability using configuration memory error detection," *IEEE Design & Test of Computers*, vol. 30, no. 2, pp. 30–39, 2013.



## International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

- [19] S. Habinc, "Functional triple modular redundancy (FTMR) for fault tolerance in FPGA designs," European Space Agency Report, 2002.
- [20] M. Caffrey, P. Graham, E. Johnson, N. Rollins, and M. Wirthlin, "Single-event upset mitigation techniques for SRAM-based FPGAs," IEEE Transactions on Nuclear Science, vol. 50, no. 6, pp. 2030–2036, 2003.
- [21]. Chithirai Pon Selvan, S.D.Vijayakumar, R. Praveenkumar, K.Sumathi, G Sekar, A Satheesh Kumar, & P. Karunakaran. (2026). An Intelligent QoS-Driven Energy-Efficient Routing Protocol for Improving Stability and Lifetime of MANETs. National Journal of Antennas and Propagation, 205-217.
- [22]. P.Arockia Mary, R.Praveenkumar, S.D. Vijayakumar, R.Jayanthi, G.Brinda, P.Jaisankar, & P.Karunakaran. (2026). Intelligent Delay-Sensitive Routing Framework for Enhanced Quality of Service in Mobile Ad Hoc Networks. National Journal of Antennas and Propagation, 167-176.
- [23]. Shanmugham, M., Sekar, G., Kavitha, S., Vijayakumar, S.D., Chithirai Pon Selvan, M. (2026). Integrating Bioacoustic Sensors for Improved Human–Computer Interaction. In: Subbaraj, K., Balusamy, B., Chithirai Pon Selvan, M., Anish Mon, F., Prabha, C. (eds) Computational Bioacoustic Artificial Intelligence. Sustainable Artificial Intelligence-Powered Applications. Springer, Cham. [https://doi.org/10.1007/978-3-032-06088-4\\_11](https://doi.org/10.1007/978-3-032-06088-4_11)
- [24] P.Arockia Mary, R.Praveenkumar, S.D. Vijayakumar, R.Jayanthi, G.Brinda, P.Jaisankar, & P.Karunakaran. (2026). Intelligent Delay-Sensitive Routing Framework for Enhanced Quality of Service in Mobile Ad Hoc Networks. National Journal of Antennas and Propagation, 167-176.
- [25] V Karthi, S.D.Vijayakumar, T.Velmurugan, Baskaran.D, G Sekar, Rajalashmi K, & Arulmozhi P. (2026). Intelligent Cross-Layer Routing Using Trust-Integrated Multi-Agent Actor–Critic Reinforcement Learning for Hybrid IoT Systems. National Journal of Antennas and Propagation, 157-166.
- [26] M.Parvathi, T.Shanmugavadivu, J.Jenshya, Balasubramaniam C, S.D.Vijayakumar, Nanthini P, & S.B.Gopal. (2026). A Hybrid Genetic Algorithm–Based Secure Multipath Routing Protocol with Trust-Aware Clustering for Performance Optimization in MANETs. National Journal of Antennas and Propagation, 188-204. <https://doi.org/10.31838/NJAP/08.02.16>
- [27] S. D. Vijayakumar, G. Vijayakumari, R. Praveenkumar, G. Brinda, T. Velmurugan and G. Sekar, "Smart Systems for Effective Garbage Handling in Urban Waste Management," 2025 International Conference on Multi-Agent Systems for Collaborative Intelligence (ICMSCI), Erode, India, 2025, pp. 748-753, doi: 10.1109/ICMSCI62561.2025.10894576.
- [28] Vijayakumar, S. D., and S. Anbu Karuppusamy. "Energy optimized air quality monitoring with AQC-MANET for real time pollutant detection and analysis." GLOBAL NEST JOURNAL 27.9 (2025).



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